WHAT IS CLAIMED IS:

1. A timing control method for operating a synchronous memory, wherein the synchronous memory has a local data bus, a signal amplification bus, and a global data bus, the timing control method comprising the steps of:

providing a synchronous timing such that following operations are carried out in a $(n+1)^{th}$ clock cycle of the synchronous timing;

reading and decoding the $(a+1)^{th}$ address;

pre-charging the local data bus that stores the a^{th} bath of local data into an initial value in a local data bus pre-charging period;

amplifying and transferring the a^{th} batch of global data from the signal amplification bus to the global data bus in a global data transmission period;

transferring the $(a+1)^{th}$ batch of local data to the local data bus in a non-local data bus pre-charging period;

pre-charging the signal amplification bus and the global data bus that stores the a^{th} batch of global data into an initial value in a signal amplification bus pre-charging period after temporarily storing the a^{th} batch of global data to a register; and

transferring the $(a+1)^{th}$ batch of local data from the local data bus to the signal amplification bus.

2. The method of claim 1, wherein the following operations are carried out in the n^{th} clock cycle of the synchronous timing:

reading out an address value;

decoding the address value; and

retrieving local bus data from a location corresponding to the address provided by the decoding operation.

3. The method of claim 2, wherein the a^{th} batch of local data is put on the local data bus in the non-local data bus pre-charging period after the address value is decoded, a column select is within the address value decoding termination cycle and other signals corresponding to the column select is within the address value decoding termination cycle.

4. The method of claim 1, wherein after the transfer of the a^{th} batch of global data from the signal amplification bus to the global data bus, further includes storing the a^{th} batch of global data in a register within the synchronous memory.

5. The method of claim 4, wherein after the transfer of the a^{th} batch of global data into the register, further includes outputting the a^{th} batch of global data from the register in the $(n+2)^{th}$ cycle of the synchronous timing.

6. The method of claim 1, wherein the step of putting the $(a+1)^{th}$ batch of local data on the local data bus requires a signal developing time for transforming the $(a+1)^{th}$ batch of local data into the $(a+1)^{th}$ batch of local data pair.

7. The method of claim 6, wherein length of the signal developing time is the period between the transition of the local data bus pre-charging period into the non-local data bus pre-charging period and the transition from the non-global data transmission period into the global data transmission period.